

Fig. 1

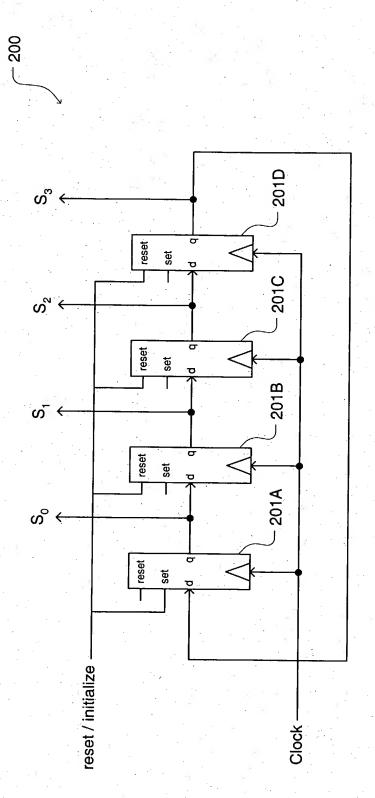


Fig. 2

1. 					Clock	Clock Cycle				0
	0	1	7	3	4	S	9	2	8	6
	1			* · · · · · · · · · · · · · · · · · · ·						
	•		•							
် လ	+	0	0	0	of	0	0	0	•	0
လ်	0	, m	0	0	0	. -	0	0	0	1
S ₂	0	0	1	0	0	0	9	0	0	0
လိ	0	0	0	1	0	0	0		0	0
Swd/SRo	{0001}	{0010}	{0100}	{1000}	{0001}	{0010}	{0100}	{1000}	{0001}	{0010}
Sw1/SR1	{1000}	{0001}	{0010}	{0100}	{1000}	{0001}	{0010}	{0100}	{1000}	{0001}
Sw2/SR2	{0100}	{1000}	{0001}	{0010}	{0100}	{1000}	{0001}	{0010}	{0100}	{1000}
S _{w3} /S _{R3}	{0010}	{0100}	{1000}	{0001}	{0010}	{0100}	{1000}	{0001}	{0010}	{0100}

Fig. 3



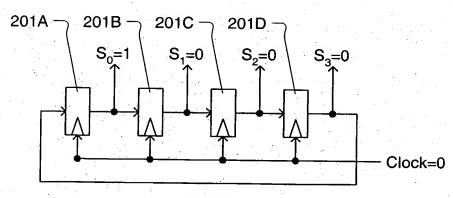


Fig. 4A

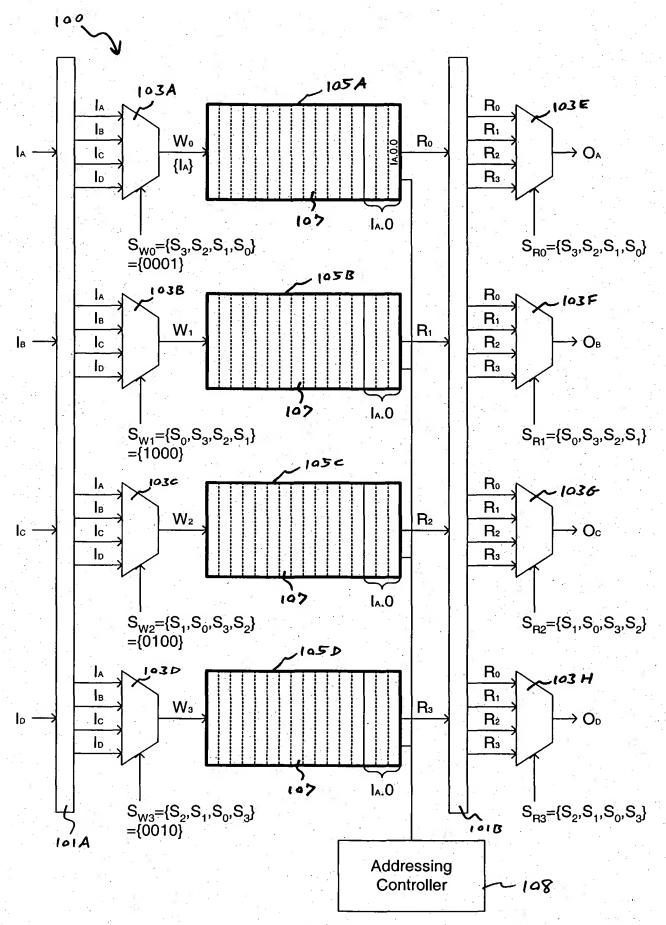


Fig. 4B



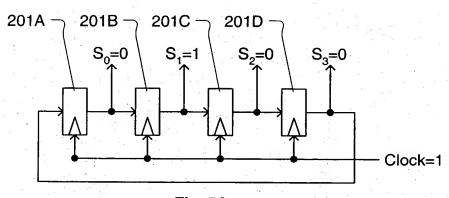


Fig. 5A

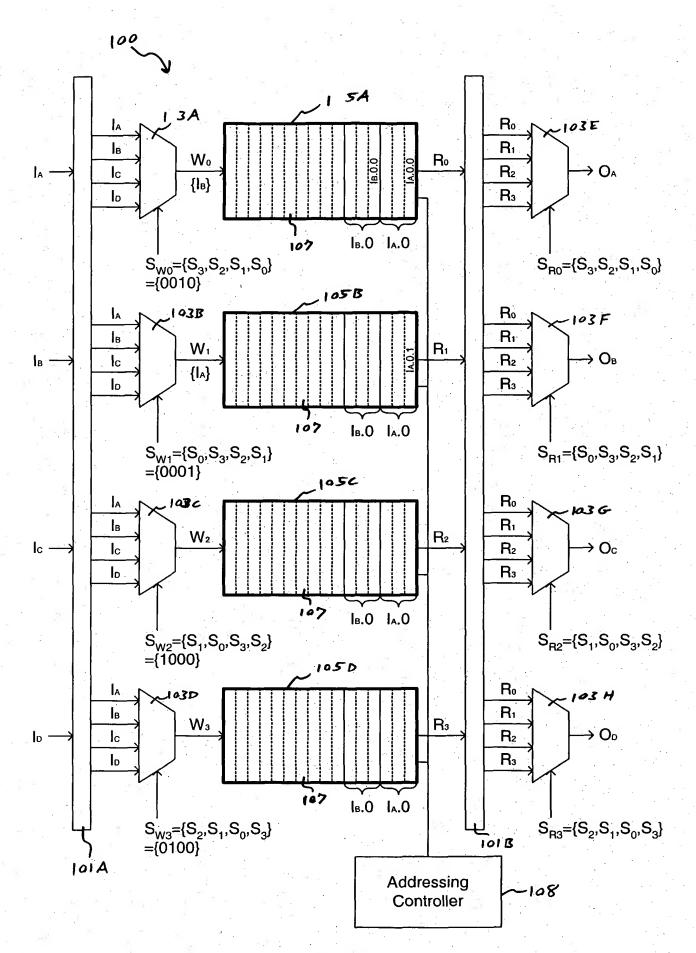


Fig. 5B



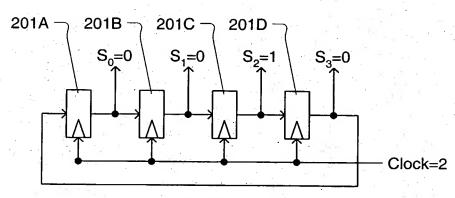


Fig. 6A

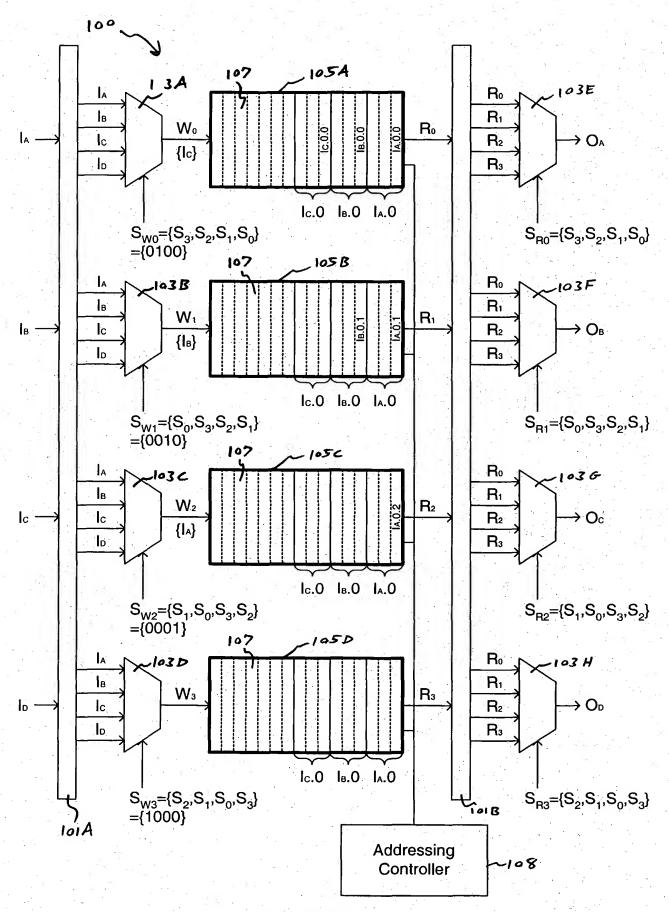


Fig. 6B



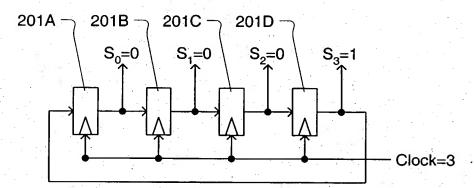


Fig. 7A

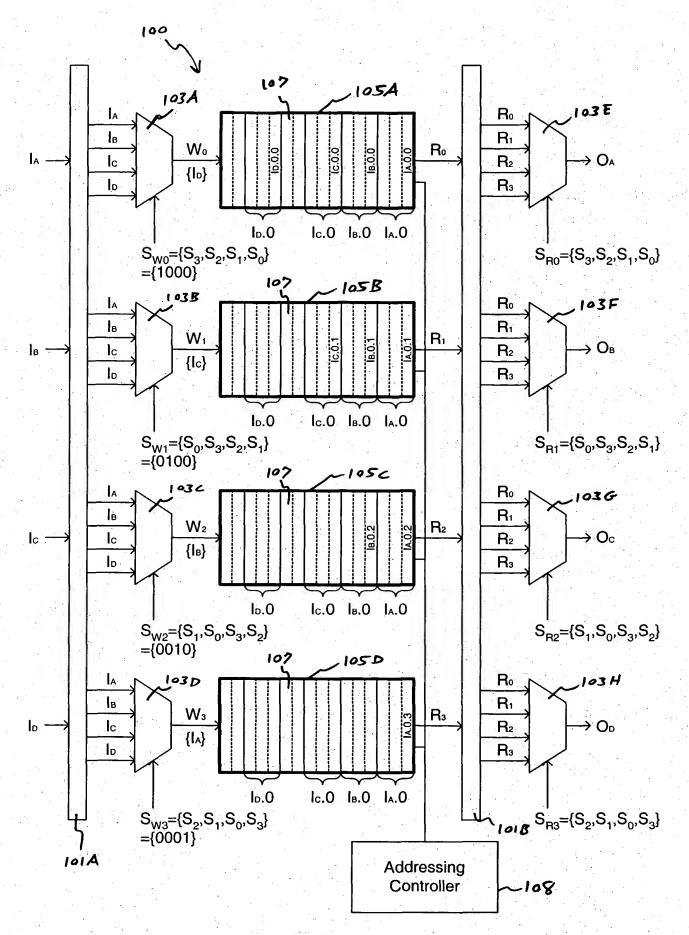


Fig. 7B



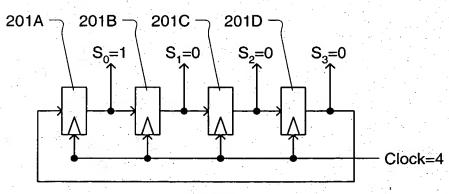


Fig. 8A

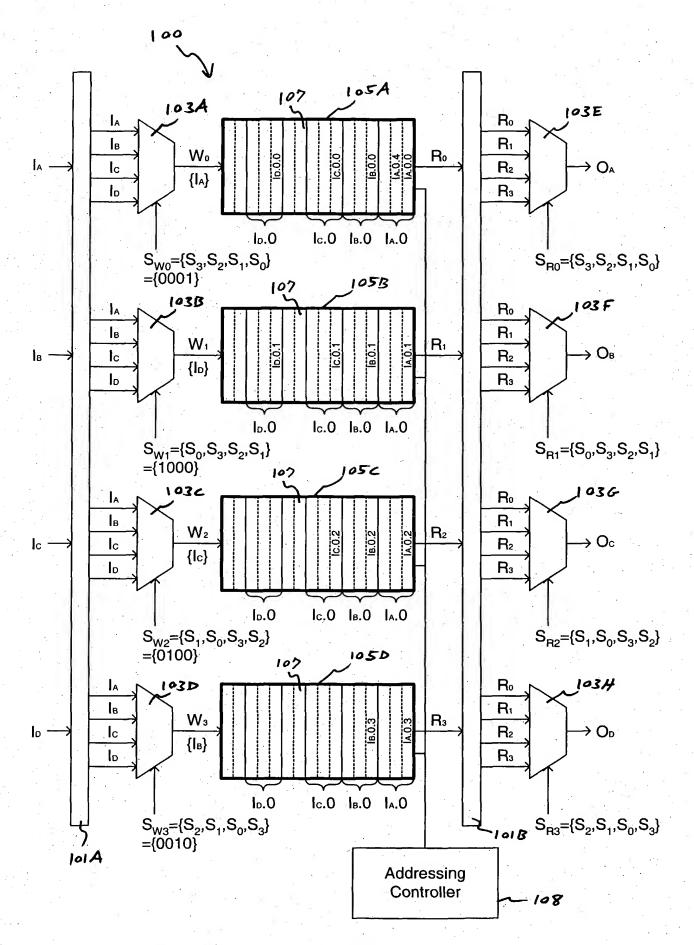
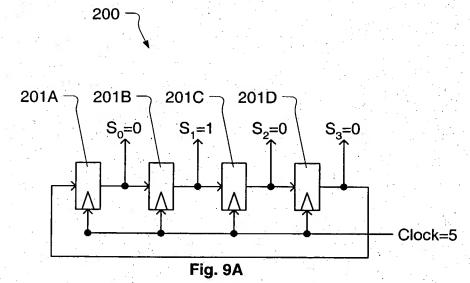


Fig. 8B



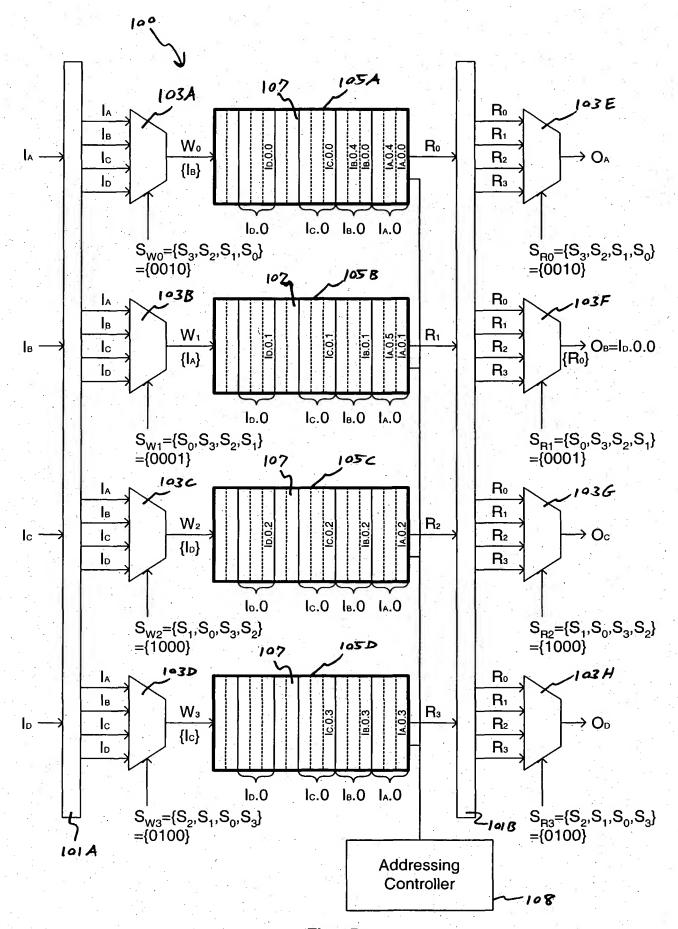
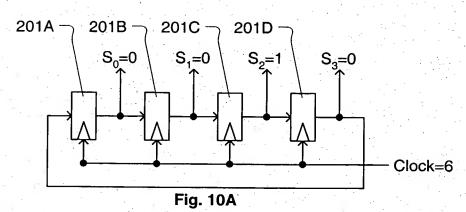


Fig. 9B





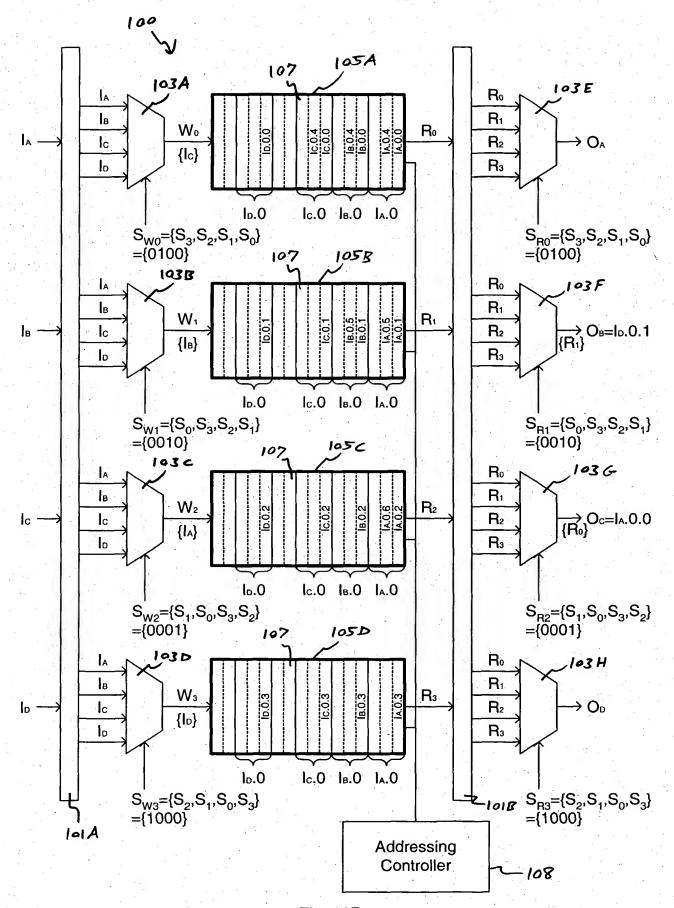


Fig. 10B



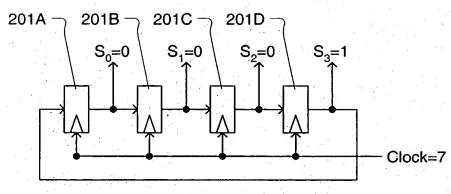


Fig. 11A

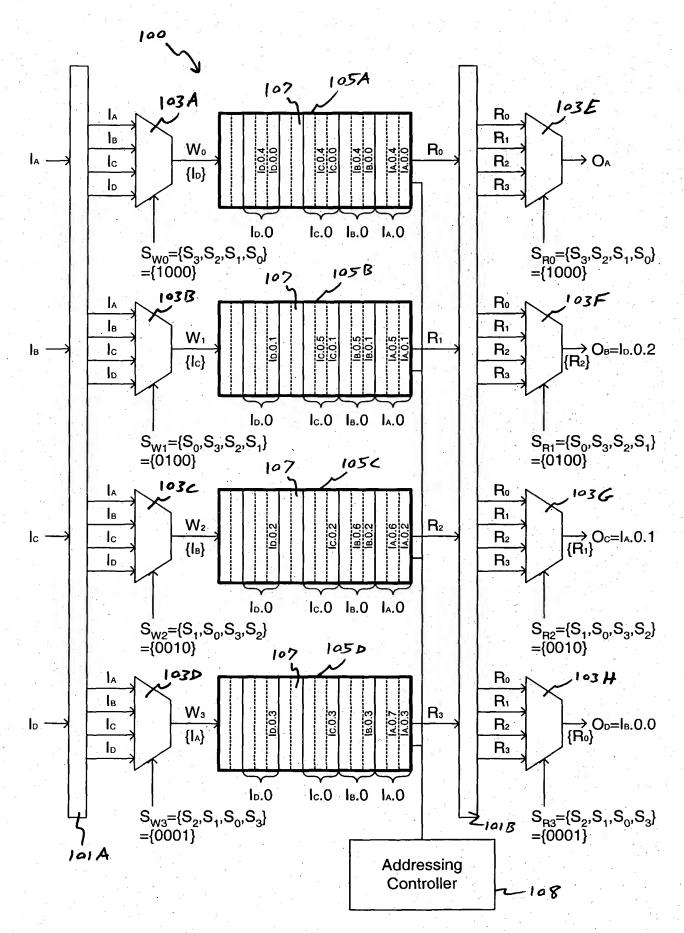
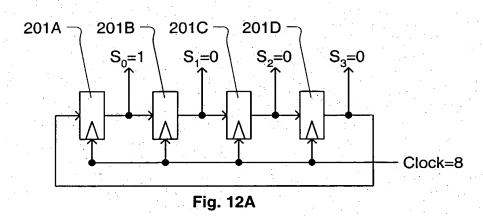


Fig. 11B





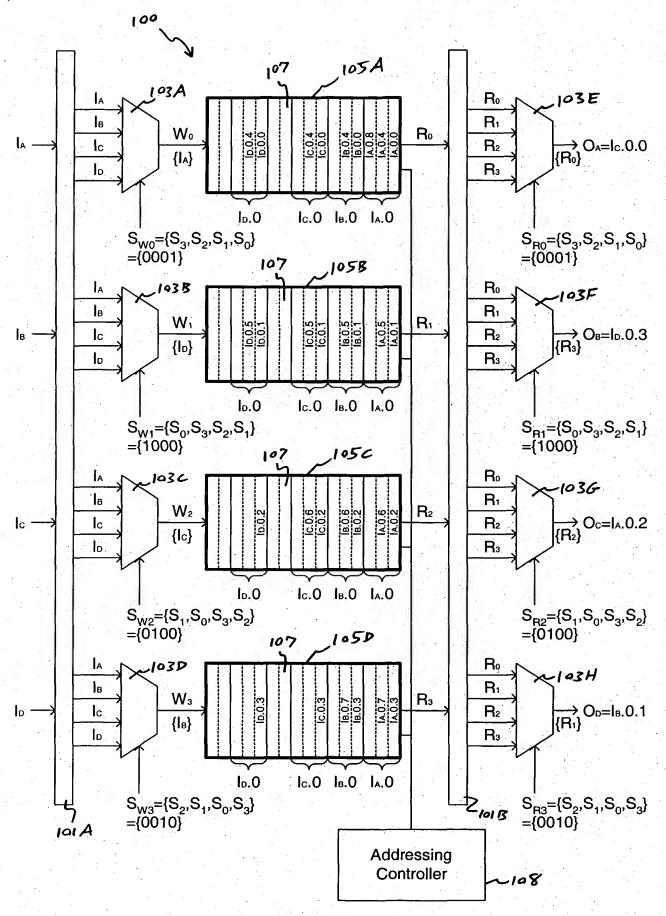


Fig. 12B



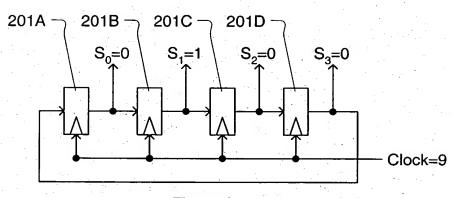


Fig. 13A

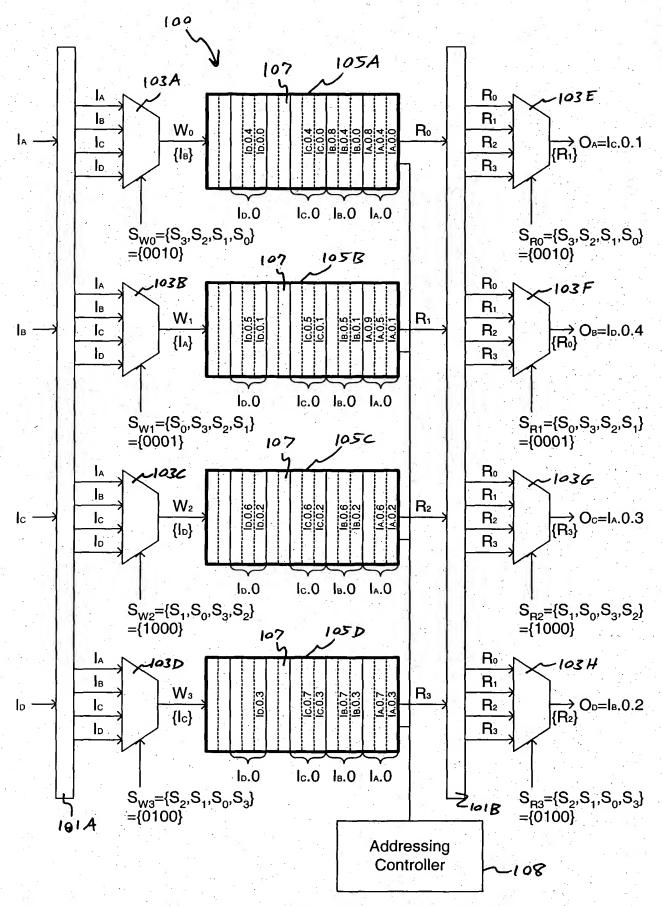


Fig. 13B

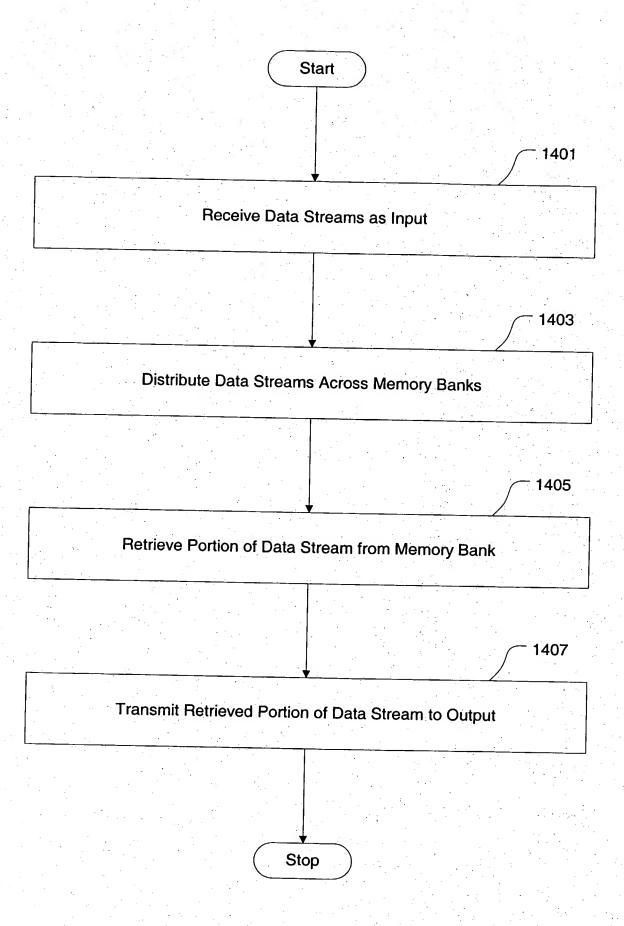


Fig. 14